## REMARKS

Reconsideration is respectfully requested.

The Specification is objected to for containing informalities. The Specification is now corrected as suggested by the Examiner to remove the informalities. A marked-up copy of the amended Specification is attached hereto. No new matter has been added.

Claims 1-9 are currently pending in the present application. By the present amendment, Claims 1 and 4-9 are amended. A marked-up copy of the amended claims is attached hereto. No new matter has been added.

Claims 1-3, 5-6, and 8-9 stand rejected under 35 U.S.C. §112, ¶2 as being indefinite for failure to particularly point and distinctly claim the subject matter which the Applicants regard as the invention. More specifically, the Examiner indicated that the term "high selection ratio" in Claim 1 is subjective.

In response, the preamble of Claim 1 has been amended to recite "A method of forming gates in a semiconductor having a non-linear profile." The support for this amendment is found in Specification page 13, lines 20-24 and page 14, lines 1-6 and also in Figs. 3D-3F.

Further, Claims 1 and 4 have been amended to include "a first high selection ratio" that is "sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers." The support for this amendment, especially with respect to the "first

high selection ratio," is found in Fig. 3D and Specification page 11, lines 11-24 and page 12, line 1.

In addition, Claims 1 and 7 have been amended to include "a second high selection ratio" that is "sufficient to polish the metal layer but insufficient to polish the insulating layer." The support for this amendment, especially with respect to the "second high selection ratio" is found in Fig. 3F and Specification page 12, lines 21-24 and page 13, lines 1-24.

The Applicants believe that the above claim amendments overcome the rejection of Claims 1-3, 5-6, and 8-9 under §112, ¶2 or §103(a). As disclosed in the Specification, the surface of the semiconductor is polished by the chemical mechanical polishing (CMP) process utilizing the appropriate high selection ratios to produce a non-linear or "wave-like" profile of the semiconductor device (Specification page 13, lines 20-24; page 14, lines 1-6). This claimed invention overcomes the problems associated with the prior art disclosed in the Background (mainly the description with respect to Fig. 2) of the present application. Therefore, the Applicants respectfully submit that Claim 1, as amended, is neither anticipated by nor obvious in view of the admitted prior art and respectfully request an indication thereof.

Claims 2-7 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Applicants' admitted prior art and further in view of U.S. Patent No. 5,356,833 (Maniar et al.).

In response, the Applicants respectfully submit that Claim 1, now amended, is not taught or suggested in the admitted prior art or Maniar et al., alone or in combination. That is, the Applicants claim, inter alia, two

exposing steps utilizing the first and second high selection ratios to carry out CMP processes. The oxide layer CMP utilizes the first high selection ratio that is sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers. The metal CMP process utilizes the second high selection ratio that is sufficient to polish the metal layer but insufficient to polish the insulating interlayer. The claimed exposing steps utilizing the first and second high selection ratios solves problems that are associated with prior art employing a general CMP process that completely planarizes an entire semiconductor surface regardless of the field and active areas on the semiconductor substrate (Specification page 5, lines 13-21). Accordingly, the technique as claimed in the present invention allows the formation of gates in a semiconductor device and the resulting non-linear top profile, which varies according to the active and field regions of the semiconductor substrate, of the semiconductor device.

Maniar et al. fails to teach or suggest such claimed invention. Maniar et al. discloses a general CMP process employed to polish "A" type elements (i.e., atomic numbers of 39-41 or 57-73) or "B" type elements (i.e., atomic numbers of 45-46 or 77-78) on the semiconductor substrate while leaving the "intermetallic layer" (defined as $AB_3$) intact. This is substantially different from the present invention that discloses, inter alia, two exposing steps employing (1) the oxide layer CMP utilizing the first high selection ratio that is sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers and (2) the metal CMP utilizing the second high selection ratio that is sufficient to polish the metal layer but insufficient to polish the insulating interlayer.

Further, Maniar et al. lacks the motivation that the CMP process is performed to create a semiconductor device having a non-linear (or "wave-like") top profile. It is submitted that the question under 35 U.S.C. §103(a) is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in the art. In re Simon, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972). It is insufficient that the art disclosed components of the Applicants' claimed invention, either separately or used in other combinations. ***However, a teaching, suggestion, or incentive must exist in the references themselves to make the combination made by the inventor.*** Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1988, ***emphasis added***). As also indicated in the MPEP, the Office bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. MPEP § 2142. One of many requirements for establishing *prima facie* obviousness is that the prior art references must teach or suggest all Claim limitations. MPEP § 2143. Further, the rejection is required to show in the references themselves that there is some suggestion or motivation to modify references or to combine reference teachings. Id. The mere fact that the teaching of the prior art can be modified or combined does not establish a motivation or suggestion to combine and make the resultant combination *prima facie* obvious. Id. The prior art must suggest the desirability of the combination. MPEP §2143.01. Maniar et al. is directed to forming an intermetallic layer ($AB_3$) on a semiconductor substrate, and the disclosed CMP process is to remove the undesired excess layer (i.e., A or B) that is left after the forming the intermetallic layer. The Applicants therefore respectfully submit that Maniar et al. fails to suggest any incentive to

combination with other references and that Claim 1, as amended, is not obvious in view of either Maniar et al. or the admitted prior art, alone or in combination.

As to the Examiner's remark on page 4 of the Office Action, the Applicants respectfully submit that the support is found in the Specification page 8; page 11, lines 17-24; page 12, lines 9-10; and page 13, lines 15-16.

As to the dependent Claims 2-9, the Applicants respectfully submit that the Claims are allowable at least since it is dependent on the independent Claim 1 that is considered to be allowable.

For the reasons set forth above, the Applicants respectfully submit that the Claims 1-9, pending in this application, are in condition for allowance over the art of record. This amendment is considered to be responsive to all points raised in the Official Action. Accordingly, the Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and earnestly solicit an indication of allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

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Respectfully submitted,

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DOCKET: CU-2636

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application: Sang Ick LEE et al.

Serial No: 09/994,284

Filed: November 26, 2001

For: METHOD OF FORMING METAL GATE IN SEMICONDUCTOR DEVICE

GRP ART UNIT: 282

Ex.: T. V. Pham



**SPECIFICATION-MARKED UP VERSION**

Please amend Specification page 4, ¶2, lines15-19 as set forth below.

"Referring to FIG. [1E] 1D, the dummy gate, exposed by CMP, is removed. [A] Now referring to FIG. 1E, a gate insulating layer 8 is then formed along a surface of the resultant structure. Subsequently, a gate metal layer 9, such as a tungsten layer, is deposited on the gate insulating layer 8."

Please amend Specification page 5, ¶ 2, lines 4-12 as set forth below.

"In a semiconductor fabrication process, a device isolation process has to precede the gate electrode formation and a gate electrode line traverses active and field areas simultaneously. As shown in FIG. 2, the surface of a field oxide layer 11 is generally higher than the surface of the semiconductor substrate 1 in the active area **t** in the device isolation process. Thus, a step difference **a** shown in FIG. 2 as the gap between the top portion of the field oxide layer 11 defining the field area **h** (FIG. 2) and the top portion of the semiconductor substrate, a mid-portion of which is defined as the active area **t** is generally between 200 to 500 Å."

DOCKET: CU-2636 PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application: Sang Ick LEE et al.
Serial No: 09/994,284 GRP ART UNIT: 2823
Filed: November 26, 2001 Ex.: T. V. Pham
For: METHOD OF FORMING METAL GATE IN SEMICONDUCTOR DEVICE



## CLAIMS-MARKED UP VERSION

Claims 1-9 are currently pending in the present application.

Please amend Claims 1 and 4-9 as set forth below.

1. (Once Amended) A method of forming [a gate] gates in a semiconductor device having a non-linear top profile, the method comprising the steps of:

forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;

depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially;

patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer and the dummy gate insulating layer using the mask pattern as an etch barrier, creating a plurality of patterned dummy gate polysilicon and insulating layers each having sidewalls, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer;

forming spacers at [both] the sidewalls of the patterned dummy gate polysilicon [layer] and insulating layers;

depositing an insulating interlayer on the resultant structure after forming the spacers;

exposing a surface of the patterned dummy gate polysilicon [layer] and insulating layers by carrying out an oxide layer [CMP] chemical mechanical polishing (CMP) process [having] utilizing a first high selection ratio [against] sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon [layer] and insulating layers;

forming a damascene structure by removing the patterned dummy gate polysilicon [layer and the dummy gate] and insulating [layer] layers using the insulating interlayer as another etch barrier;

depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure; and

exposing a surface of the insulating interlayer by carrying out a metal [chemical mechanical polishing] CMP process [having] utilizing a second high selection ratio sufficient to polish the metal layer but insufficient to polish [against] the insulating interlayer.

4. (Once Amended) The method of claim 1, wherein the [polishing] first high selection ratio between the insulating interlayer and the dummy gate polysilicon layer is [maintained] over 20.

5. (Once Amended) The method of claim 1, wherein the insulating interlayer [chemical mechanical polishing uses] CMP utilizes a slurry including $CeO_2$ particles.

6. (Once Amended) The method of claim 5, wherein the pH of the slurry, including $CeO_2$ particles, is [set] between 3 and 11.

7. (Once Amended) The method of claim 1, wherein the [polishing] second high selection ratio between the insulating interlayer and the gate metal layer is [maintained] over 50.

8. (Once Amended) The method of claim 1, wherein the metal [chemical mechanical polishing] CMP uses a slurry for [a] the metal layer.

9. (Once Amended) The method of claim 8, wherein the pH of the slurry for [a] the metal layer is [set] between 2 and 7.